COMPOSITE FIELD EFFECT TRANSISTOR

CROSS-REFERENCE TO RELATED APPLICATIONS

This application claims the benefit of U.S. Provisional Application No. 60/663,315 filed Mar. 18, 2005.

BACKGROUND OF THE INVENTION

Depletion mode junction field effect transistors (JFETs) are efficient semiconductor structures, especially for high-voltage switching applications. However, depletion mode JFETs require a negative gate-to-source potential to turn off. Accordingly, when a system incorporating a JFET is first turned on, the depletion mode JFET is also on, causing undesirable high current to flow in most applications.

An enhancement mode metal-oxide-semiconductor field effect transistor (MOSFET), on the other hand, requires a positive voltage to turn on. Therefore, the MOSFET, being a normally off device, does not typically exhibit high current flows in most applications upon start-up. However, MOSFETs are generally not normally the most cost-efficient devices for high voltage (>100V) applications.

Accordingly, there remains a need for semiconductor device having C) improved high-voltage switching characteristics in combination with low current flow characteristics at start-up and no requirement for negative gate bias.

SUMMARY OF THE INVENTION

Embodiments of the present invention provide a composite field effect transistor that includes a zener diode, a junction field effect transistor and a metal-oxide-semiconductor field effect transistor. A gate of the junction field effect transistor is coupled to an anode of the zener diode. A cathode of the zener diode is coupled to a gate of the metal-oxide-semiconductor field effect transistor. A drain of the metal-oxide-semiconductor field effect transistor is coupled to a source of the junction field effect transistor. In one implementation, the junction field effect transistor is a depletion mode device and the metal-oxide-semiconductor field effect transistor is an n-channel enhancement mode device.

BRIEF DESCRIPTION OF THE DRAWINGS

Embodiments of the present invention are illustrated by way of example and not by way of limitation, in the figures of the accompanying drawings and in which like reference numerals refer to similar elements and in which:

FIG. **1** shows a diagram of a composite field effect transistor (FET), in accordance with one embodiment of the invention.

FIG. **2** shows a diagram of a composite FET, in accordance with another embodiment of the invention.

DETAILED DESCRIPTION OF THE INVENTION

Reference will now be made in detail to the embodiments of the invention, examples of which are illustrated in the accompanying drawings. While the invention will be described in conjunction with these embodiments, it will be understood that they are not intended to limit the invention to these embodiments. On the contrary, the invention is intended to cover alternatives, modifications and equivalents, which may be included within the scope of the invention as defined by the appended claims. Furthermore, in the following detailed description of the present invention, numerous specific details are set forth in order to provide a thorough understanding of the present invention. However, it is understood that the present invention may be practiced without these specific details. In other instances, well-known methods, procedures, components, and circuits have not been described in detail as not to unnecessarily obscure aspects of the present invention.

FIG. **1** shows a diagram of a composite field effect transistor (FET) **100** having a gate, drain and source, in accordance with one embodiment of the invention. The composite FET **100** includes a depletion mode junction field effect transistor (JFET) **110** (Q**1**), an enhancement mode N-channel metal-oxide-semiconductor field effect transistor (MOSFET) **120** (Q**2**) and a zener diode **130** (CR**1**). The drain of the JFET **110** is coupled to the drain of the composite FET **100**. The source of the JFET **110** is coupled to the drain of the MOSFET **120**. The source of the MOSFET **120** is coupled to the source of the composite FET **100**. The anode of the zener diode **130** is coupled to the gate of the JFET **110** and the cathode of the zener diode **130** is coupled to the gate of the MOSFET **120**. The gate of the MOSFET **120** is also coupled to the gate of the composite FET **100**.

When the gate-to-source potential of the composite FET **100** is less than the threshold voltage ($V_{T(Q2)}$) of the MOSFET **120**, the MOSFET **120** is turned off and blocks current from flowing between the source and drain of the composite FET **100**. When the gate-to-source potential of the composite FET **100** is greater than the threshold voltage of the MOSFET **120** and less than the breakdown voltage of the zener diode **130**, the MOSFET **120** will turn on pulling the source of the JFET **100** down. However, the zener diode **130** blocks the potential at the gate of the JFET **110** and therefore the JFET **110** remains off.

When the gate-to-source potential of the composite FET **100** reaches the threshold voltage of the JFET **110** plus the breakdown voltage of the zener diode **130** ($V_{GS(Q1)}+V_{Z(CR1)}$), both the JFET **110** and MOSFET **120** are turned on and current is conducted between the source and drain of the composite FET **100**. In addition, when the gate-to-source potential of the composite FET **100** reaches the threshold voltage of the JFET **110** plus the breakdown voltage of the zener diode **130** ($V_{GS(Q1)}+V_{Z(CR1)}$), current-flowing through the zener diode **120** acts to inject minority carriers into the JFET **110**, thereby improving its conductivity of the composite FET **100** especially at high drain currents.

When the gate-to-source potential of the composite FET **100** pulls low, the zener diode **130** conducts in its forward direction and simultaneously pulls the gate potential of the JFET **110** negative while the gate potential of MOSFET **120** is being pulled negative. As a result, the MOSFET **120** begins to turn off. As MOSFET **120** turns off, its drain potential rises, causing the gate-to-source voltage of the JFET **110** to be negative, which in turn causes the JFET **110** to turn off completely, blocking current from flowing between the source and drain of the composite FET **100**.

FIG. **2**, shows a diagram of a composite FET **200**, in accordance with another embodiment of the invention. The composite FET **200** is illustrated coupled to a high voltage source **220** and an external drive circuit **220**. The high voltage source **210** is coupled to the drain of the composite FET **200**. The external drive circuit **220** is coupled to the gate of the composite FET **200**.